EXHIBIT A

US006946371B2

(12) **United States Patent**
Langdo et al.

(10) **Patent No.: US 6,946,371 B2**
(45) **Date of Patent: Sep. 20, 2005**

(54) **METHODS OF FABRICATING SEMICONDUCTOR STRUCTURES HAVING EPITAXIALLY GROWN SOURCE AND DRAIN ELEMENTS**

(75) Inventors: **Thomas A. Langdo**, Cambridge, MA (US); **Anthony J. Lochtefeld**, Somerville, MA (US)

(73) Assignee: **Amberwave Systems Corporation**, Salem, NH (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 22 days.

(21) Appl. No.: **10/458,544**

(22) Filed: **Jun. 10, 2003**

(65) **Prior Publication Data**

US 2004/0045499 A1 Mar. 11, 2004

Related U.S. Application Data

(60) Provisional application No. 60/387,867, filed on Jun. 10, 2002.

(51) **Int. Cl.**[7] **H01L 21/20**

(52) **U.S. Cl.** **438/481**; 438/504

(58) **Field of Search** 438/481, 504, 438/505

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,717,681 A	1/1988	Curran	
4,755,478 A	7/1988	Abernathey et al.	437/41
4,803,539 A	2/1989	Psaras et al.	
5,034,348 A	7/1991	Hartswick et al.	
5,089,872 A	2/1992	Ozturk et al.	
5,198,689 A	3/1993	Fujioka	
5,217,923 A	6/1993	Suguro	
5,242,847 A	9/1993	Ozturk et al.	
5,334,861 A	8/1994	Pfiester et al.	
5,336,903 A	8/1994	Ozturk et al.	
5,346,840 A	9/1994	Fujioka	
5,442,205 A	8/1995	Brasen et al.	
5,496,750 A	3/1996	Moslehi	
5,496,771 A	3/1996	Cronin et al.	437/187
5,659,194 A	8/1997	Iwamatsu et al.	

(Continued)

FOREIGN PATENT DOCUMENTS

JP	2002-324765	11/2002
WO	WO01/22482	3/2001
WO	02/13262 A2	2/2002

OTHER PUBLICATIONS

Antoniadis et al., "SOI Devices and Technology," *SOI devices and technology*, Neuilly sur Seine, France, 1999, pp. 81–87.

Aoyama et al., "Facet formation mechanism of silicon selective epitaxial layer by Si ultrahigh vacuum chemical vapor deposition," *Journal of Crystal Growth*, 136 (1994), pp. 349–354.

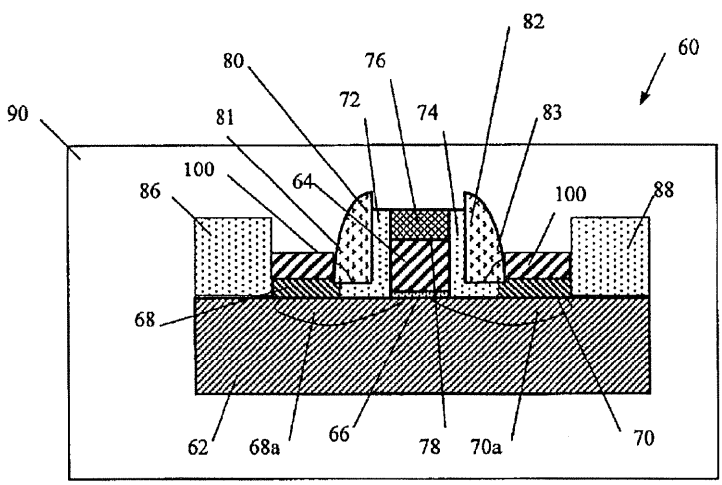
(Continued)

Primary Examiner—George Fourson
Assistant Examiner—Fernando L. Toledo
(74) *Attorney, Agent, or Firm*—Goodwin Procter, LLP

(57) **ABSTRACT**

Methods for fabricating facetless semiconductor structures using commercially available chemical vapor deposition systems are disclosed herein. A key aspect of the invention includes selectively depositing an epitaxial layer of at least one semiconductor material on the semiconductor substrate while in situ doping the epitaxial layer to suppress facet formation. Suppression of faceting during selective epitaxial growth by in situ doping of the epitaxial layer at a predetermined level rather than by manipulating spacer composition and geometry alleviates the stringent requirements on the device design and increases tolerance to variability during the spacer fabrication.

35 Claims, 5 Drawing Sheets



U.S. PATENT DOCUMENTS

5,714,777	A	2/1998	Ismail et al.	
5,844,260	A	12/1998	Ohori	257/190
5,847,419	A	12/1998	Imai et al.	
5,869,359	A	2/1999	Prabhakar	
5,877,535	A	3/1999	Matsumoto	257/369
5,891,769	A	4/1999	Liaw et al.	438/167
5,933,741	A	8/1999	Tseng	
5,998,807	A	12/1999	Lustig et al.	
6,008,111	A	12/1999	Fushida et al.	
6,066,563	A	5/2000	Nagashima	
6,096,647	A	8/2000	Yang et al.	
6,107,653	A	8/2000	Fitzgerald	
6,121,100	A	9/2000	Andideh et al.	
6,132,806	A	10/2000	Dutartre	
6,133,124	A	10/2000	Horstmann et al.	
6,159,856	A	12/2000	Nagano	
6,187,657	B1	2/2001	Xiang et al.	438/596
6,214,679	B1	4/2001	Murthy et al.	
6,235,575	B1	5/2001	Kasai et al.	
6,246,077	B1	6/2001	Kobayashi et al.	257/77
6,251,780	B1	6/2001	Sohn et al.	
6,268,257	B1	7/2001	Wieczorek et al.	
6,281,532	B1	8/2001	Doyle et al.	
6,291,321	B1	9/2001	Fitzgerald	438/494
6,294,448	B1	9/2001	Chang et al.	
6,306,698	B1	10/2001	Wieczorek et al.	
6,313,486	B1	11/2001	Kencke et al.	257/192
6,315,384	B1	11/2001	Ramaswami et al.	
6,316,357	B1	11/2001	Lin et al.	
6,319,805	B1	11/2001	Iwamatsu et al.	
6,362,071	B1	3/2002	Nguyen et al.	
6,380,008	B2	4/2002	Kwok et al.	
6,399,970	B2	6/2002	Kubo et al.	
6,406,986	B1	6/2002	Yu	
6,410,371	B1	6/2002	Yu et al.	
6,461,960	B2	10/2002	Lee	
6,486,520	B2	11/2002	Okuno et al.	
6,498,359	B2	12/2002	Schmidt et al.	
6,503,833	B1	1/2003	Ajmera et al.	
6,509,587	B2	1/2003	Sugiyama et al.	
6,555,839	B2	4/2003	Fitzgerald	
6,555,880	B2	4/2003	Cabral et al.	
6,562,703	B1 *	5/2003	Maa et al.	438/518
6,563,152	B2	5/2003	Roberds et al.	
6,566,718	B2	5/2003	Wieczorek et al.	
6,573,126	B2	6/2003	Chen et al.	
6,573,160	B2	6/2003	Taylor, Jr. et al.	
6,583,015	B2	6/2003	Fitzgerald et al.	
6,593,191	B2	7/2003	Fitzgerald	
6,593,641	B1	7/2003	Fitzgerald	
6,603,156	B2	8/2003	Rim	
6,605,498	B1	8/2003	Murthy et al.	
6,621,131	B2	9/2003	Murthy et al.	
6,657,223	B1	12/2003	Wang et al.	
6,682,965	B1	1/2004	Noguchi et al.	
6,686,617	B2	2/2004	Agnello et al.	
6,699,765	B1 *	3/2004	Shideler et al.	438/312
6,703,648	B1	3/2004	Xiang et al.	
6,724,019	B2	4/2004	Oda et al.	
6,743,684	B2	6/2004	Liu	
2001/0001724	A1	5/2001	Kwok et al.	
2001/0009303	A1	7/2001	Tang et al.	
2001/0031535	A1	10/2001	Agnello et al.	
2001/0045604	A1	11/2001	Oda et al.	
2002/0019127	A1	2/2002	Givens	
2002/0048910	A1	4/2002	Taylor, Jr. et al.	
2002/0052084	A1	5/2002	Fitzgerald	
2002/0056879	A1	5/2002	Wieczorek et al.	
2002/0063292	A1	5/2002	Armstrong et al.	
2002/0190284	A1	12/2002	Murthy et al.	
2003/0113971	A1 *	6/2003	Nagaoka et al.	438/287
2004/0007724	A1	1/2004	Murthy et al.	
2004/0014276	A1	1/2004	Murthy et al.	
2004/0014304	A1	1/2004	Bhattacharyya	
2004/0070035	A1	4/2004	Murthy et al.	
2004/0084735	A1	5/2004	Murthy et al.	
2004/0119101	A1	6/2004	Schrom et al.	
2004/0142545	A1	7/2004	Ngo et al.	
2004/0173815	A1	9/2004	Yeo et al.	

OTHER PUBLICATIONS

Arst et al., "Surface planarity and microstructure of low temperature silicon SEG and ELO," *Journal of Materials Research*, vol. 6, No. 4 (Apr. 1991), pp. 784–791.

Cao et al., "0.18–μm Fully–Depleted Silicon–on–Insulator MOSFET's," *IEEE Electron Device Letters*, vol. 18, No. 6 (Jun. 1997), pp. 251–253.

Chieh et al., "Low–Resistance Bandgap–Engineered W/$Si_{1-x}Ge_x$/Si Contacts," *IEEE Electron Device Letters*, vol. 17, No. 7 (Jul. 1996), pp. 360–362.

Choi et al., "Nanoscale Ultrathin Body PMOSFETs With Raised Selective Germanium Source/Drain," *IEEE Electron Device Letters*, vol. 22, No. 9 (Sep. 2001), pp. 447–448.

Choi et al., "30nm ultra–thin body SOI MOSFET with selectively deposited Ge raised S/D," *58th Device Research Conference* (2000), pp. 23–24.

Drowley et al., "Model for facet and sidewall defect formation during selective epitaxial growth of (001) silicon," *Applied Physics Letters*, 52 (7) (Feb. 15, 1988), pp. 546–548.

Eaglesham et al., "Growth Morphology and the Equilibrium Shape: The Role of "Surfactants" in the Ge/Si Island Formation," *Physical Review Letters*, vol. 70, No. 7 (Feb. 15, 1993), pp. 966–969.

Gallas et al., "Influence of doping on facet formation at the SiO2/Si interface," *Surface Science*, 440 (1999) pp. 41–48.

Glück et al., "$CoSi_2$ and $TiSi_2$ for Si/SiGe heterodevices," *Thin Solid Films*, vol. 270 (1995), pp. 549–554.

Goulding, "The selective epitaxial growth of silicon," *Materials Science and Engineering*, B17 (1993), pp. 47–67.

Greve et al., "Growth Rate of Doped and Undoped Silicon by Ultra–High Vacuum Chemical Vapor Deposition," *Journal of the Electrochemical Society*, vol. 138, No. 6 (Jun. 1991), pp. 1744–1748.

Huang et al., "Electrical and Compositional Properties of Co–Silicided Shallow P^+–n Junction Using Si–Capped/Boron–Doped $Si_{1-x}Ge_x$ Layer Deposited by UHVCME," *Journal of the Electrochemical Society*, vol. 148, No. 3 (2001), pp. G126–G131.

Ilderem et al., "Very low pressure chemical vapor deposition process for selective titanium silicide films," *Appl. Phys. Lett.*, vol. 53, No. 8 (Aug. 22, 1988), pp. 687–689.

Ishitani et al., "Facet Formation in Selective Silicon Epitaxial Growth," *Japanese Journal of Applied Physics*, vol. 24, No. 10 (Oct., 1995), pp. 1267–1269.

Jang et al., "Phosphorus doping of epitaxial Si and Si1–xGex at very low pressure," *Applied Physics Letters*, 63 (12) (Sep. 20, 1993), pp. 1675–1677.

Jastrzebski, "SOI by CVD: Epitaxial Lateral Overgrowth (ELO) Process—Review," *Journal of Crystal Growth*, 63 (1983), pp. 493–526.

Kamins et al., "Kinetics of selective epitaxial deposition of Si1–xGex," *Applied Physics Letters*, 61 (6) (Aug. 10, 1992), pp. 669–671.

Kendel et al., "Surfactant Mediated Crystal Growth of Semiconductors," *Physical Review Letters*, vol. 75, No. 14 (Oct. 2, 1995), pp. 2742–2745.

King, "Silicon–Germanium: from Microelectronics to Micromechanics," Presentation to the Thin Film Users Group Meeting, AVS Northern California Chapter, Apr. 17, 2002.

Kitajima et al., "Lattice Defect in Selective Epitaxial Silicon and Laterally Overgrown Regions on SiO2," *Journal of Crystal Growth*, 98 (1989), pp. 264–276.

Kummer et al., "Low energy plasma enhanced chemical vapor deposition," *Materials Science and Engineering*, B89 (2002), pp. 288–295.

Langdo, "Selective SiGe Nanostructures," Ph.D. Thesis, Massachusetts Institute of Technology, 2001.

Li et al., "Modeling of facet growth on patterned Si substrate in gas source MBE," *Journal of Crystal Growth*, 157 (1995), pp. 185–189.

Lochtefeld, "Toward the End of the MOSFET Roadmap: Investigating Fundamental Transport Limits and Device Architecture Alternatives," Ph.D. Thesis, Massachusetts Institute of Technology, 2001.

Lynch, "Self–Aligned Contact Schemes for Source–Drains in Submicron Devices," *IEDM Technical Digest* (1987), pp. 354–357.

Maillard–Schaller et al., "Role of the substrate strain in the sheet resistance stability of NiSi deposited on Si(100)," *Journal of Applied Physics*, vol. 85, No. 7 (Apr. 1, 1999), pp. 3614–3618.

Maiti et al., "Strained–Si heterostructure field effect transistors," *Semiconductor Science and Technology*, vol. 13 (1998), pp. 1225–1246.

Mercier et al., "Selective $TiSi_2$ Deposition with no Silicon Substrate Consumption by Rapid Thermal Processing in a LPCVD Reactor," *Journal of Electronic Materials*, vol. 19, No. 3 (1990), pp. 253–258.

Meyerson et al., "Phosphorus–Doped Polycrystalline Silicon via LPCVD," *Journal of the Electrochemical Society*, vol. 131, No. 10 (Oct. 1984), pp. 2366–2368.

Miyano et al., "Facet–Free Si Selective Epitaxial Growth Adaptable to Elevated Source/Drain MOSFETs with Narrow Shallow Trench Isolation," *Japanese Journal of Applied Physics*, vol 38, Part 1, No. 4B (Apr. 1999), pp. 2419–2423.

Moon et al., "Application of interferometric broadband imaging alignment on an experimental x–ray stepper," *Journal of Vacuum Science and Technology*, B 16(6) (Nov./Dec. 1998), pp. 3631–3636.

Osburn et al., "Low parasitic resistance contacts for scaled ULSI devices," *Thin Solid Films*, 332 (1998), pp. 428–436.

Öztürk et al., "Rapid Thermal Chemical Vapor Deposition of Germanium and Germanium/Silicon Alloys on Silicon: New Applications in the Fabrication of MOS Transistors," *Materials Research Society Symposium Proceedings*, vol. 224 (1991), pp. 223–234.

Pfiester et al., "A Self–Aligned Elevated Source/Drain MOSFET," *IEEE Electron Device Letters*, vol. 11, No. 9 (Sep. 1990), pp. 365–367.

Raaijmakers et al., "Enabling technologies for forming and contacting shallow junctions in Si: HF–vapor cleaning and selective epitaxial growth of Si and SiGe," *Journal of Vacuum Science and Technology*, B 17(5) (Sep./Oct. 1999), pp. 2311–2320.

Ren et al., "A Novel Implantation Free Raised Source/Drain MOSFET Process Using Selective Rapid Thermal Chemical Vapor Deposition of In–Situ Boron Doped Si_x Ge_{1-x}," *Materials Research Society Symposium Proceedings*, vol. 303 (1993), pp. 37–41.

Reynolds et al., "Selective titanium disilicide by low–pressure chemical vapor deposition," *Journal of Applied Physics*, vol. 65, No. 8 (Apr. 15, 1989), pp. 3212–3218.

Robbins et al., "A model for heterogeneous growth of Si1–xGex films from hydrides," *Journal of Applied Physics*, 69 (6) (Mar. 15, 1991), pp. 3729–3732.

Rodder et al., "Raised Source/Drain MOSFET with Dual Sidewall Spacers," *IEEE Electron Device Letters*, vol. 12, No. 3 (Mar. 1991), pp. 89–91.

Samavedam et al., "Elevated source drain devices using silicon selective epitaxial growth," *Journal of Vacuum Science and Technology*, B 18(3) (May/Jun. 2000), pp. 1244–1250.

Savina et a., "Faceting of a growing crystal surface by surface diffusion," *Physical Review*, E 67, 021606 (2003), pp 1–16.

Sedgwick et al., "Growth of Facet–Free Selective Silicon Epitaxy at Low Temperature and Atmospheric Pressure," *Journal of the Electrochemical Society*, vol. 138, No. 10 (Oct. 1991), pp. 3042–3047.

Shibata et al., "High Performance Half–Micron PMOSFETs with 0.1UM Shallow P^+N Junction Utilizing Selective Silicon Growth and Rapid Thermal Annealing," *IEDM Technical Digest* (1987), pp. 590–593.

Sidek et al., "Reduction of parasitic bipolar transistor action and punchthrough susceptibility in MOSFETs using Si/Si1–xGex sources and drains," *Electronics Letters*, vol. 32, No. 3 (Feb. 1, 1996), pp. 269–270.

Sun et al., "A Comparative Study of n+/p Junction Formation for Deep Submicron Elevated Source/Drain Metal Oxide Semiconductor Field Effect Transistors," *Journal of the Electrochemical Society*, vol. 144, No. 10 (Oct. 1997), pp. 3659–3664.

Sun et al., "The Effect of the Elevated Source/Drain Doping Profile on Performance and Reliability of Deep Submicron MOSFET's," *IEEE Transactions on Electron Devices*, vol. 44, No. 9 (Sep. 1997), pp. 1491–1498.

Sun et al., "Impact of Epi Facets on Deep Submicron Elevated Source/Drain MOSFET Characteristics," *IEEE Transactions on Electron Devices*, vol. 45, No. 6 (Jun. 1998), pp. 1377–1380.

Tromp et al., "Local Dimer Exchange in Surfactant–Mediated Epitaxial Growth," *Physical Review Letters*, vol. 68, No. 7 (Feb. 17, 1992), pp. 954–957.

Uchino et al., "MOSFETs with Ultrashallow Junction and Minimum Drain Area Formed by Using Solid–Phase Diffusion from SiGe," *IEEE Transactions on Electron Devices*, vol. 48, No. 7 (Jul. 2001), pp. 1406–1411.

Uhrberg et al., "Electronic and atomic structure of arsenic terminated Si(100)," *Journal of Vacuum Science and Technology*, A 4 (3) (May/Jun. 1986), pp. 1259–1264.

Violette et al., "Facet–Free Selective Silicon Epitaxy by Reduced–Pressure Chemical Vapor Deposition: Process Evaluation and Impact on Shallow Trench Isolation," *Journal of the Electrochemical Society*, 146 (5) (1999), pp. 1895–1902.

Wong et al., "Elevated Source/Drain MOSFET," *IEDM Technical Digest*, 28 (1984), pp. 634–637.

Xiang et al., "Interfacet mass transport and facet evolution in selective epitaxial growth of Si by gas source molecular beam epitaxy," *Journal of Vacuum Science and Technology*, B 14(3) (May/Jun. 1996), pp. 2381–2386.

Yu et al., "Doping reaction of PH3 and B2H6 with Si(100)," *Journal of Applied Physics*, 59 (12) (Jun. 15, 1986), pp. 4032–4037.

Augendre et al., "Elevated Source/Drain by Sacrificial Selective Epitaxy for High Performance Deep Submicron CMOS: Process Window versus Complexity," *IEEE Transactions on Electron Devices*, vol. 47, No. 7 (Jul. 2000), pp. 1484–1491.

International Search Report for PCT/US03/18140, Nov. 5, 2003, 5 pages.

Meyer, "Elevated Source/Drain Structures," *The ASM Epitaxy Newsletter of Continuous Improvement*, (Spring 1998).

Yew, "Growth and Characterization of Low Temperature Silicon Selective Epitaxy," Ph.D. Thesis, MIT, 1990, pp. 1–210.

Kurosawa et al., "A New Bird's Beak Free Field Isolation Technology for VLSI Devices," *IEDM Technical Digest*, Washington, D.C., Dec. 7–9, 1981, pp. 384–387.

O'Neill et al., "Si–Ge Virtual Substrate N–channel Heterojunction MOSFETs", *Semiconductor Science Technology*, vol. 14, No. 9, 1999, pp. 784–789.

Aldrich et al., "Stability of C54 Titanium Germanosilicide on a Silicon–Germanium Alloy Substrate," *J. Appl. Phys.*, 1995, 77(10):5107–5114.

Aubry–Fortuna et al., "Phase Formation and Strain Relaxation During Thermal Reaction of Zr and Ti with Strained $Si_{1-x-y}Ge_xC_y$ epilayers," *Journal of Applied Physics*, 2000, 88(3):1418–1423.

Detavernier, et al., "$CoSi_2$ Nucleation in the presence of Ge," *Thin Solid Films*, 2001, 384(2):243–250.

Eberhardt et al., "Ni/Ag Metallization for SiGe HBTs using a Ni Silicide Contact," *Semicond. Sci. Technol.*, 2001 16(9):L47–L49.

Freiman et al., "Kinetics of Processes in the Ti–$Si_{1-x}Ge_x$ Systems," *Appl. Phys. Lett.*, 1996, 69(25):3821–3823.

Freiman et al., "Titanium Metallization of Si/Ge Alloys and Superlattices," *Thin Solid Films*, 1997, 294:217–219.

Hsiao et al., "Advanced Technologies for Optimized Sub–Quarter–Micrometer SOI CMOS Devices," *IEEE Transactions on Electron Devices*, 1998, 45(5):1092–1098.

Huang et al., "Study on Ge/Si ratio, Silicidation, and Strain Relaxation of High Temperature Sputtered Co/$Si_{1-x}Ge_x$ Structures," *Journal of Applied Physics*, 2000, 88(4):1831–1837.

Jungemann et al., "Full–Band Monte Carlo Simulation of a 0.12 μm–Si–PMOSFET with and without a Strained SiGe–Channel", *IEEE Electron Devices Meeting*, 1998, pp. 897–900.

King et al., "A Polycrystalline $Si_{1-x}Ge_x$–Gate CMOS Technology", *IEEE*, vol., No., 1990, pp. 253–256.

Ku et al., "High Performance pMOSFETs with Ni(Si_xGe_{1-x})/Poly–$Si_{0.8}Ge_{0.2}$ Gate," *IEEE—2000 Symposium on VLSI Technology Digest of Technical Papers*, 2000, 114–115.

Lai et al., "Effects of Composition on the Formation Temperatures and Electrical Resistivities of C54 Titanium Germanosilicide in Ti–$Si_{1-x}Ge_x$ Systems," 1999, *Journal of Applied Physics*, 86(3):1340–1345.

Okada et al., "Epitaxial Growth of Heavily B–Doped SiGe Films and Interfacial Reaction of Ti/B–Doped SiGe Bilayer Structure Using Rapid Thermal Processing," *Thin Solid Films*, 2000, 369:130–133.

Qin et al., "Structure and Thermal Stability of Ni/$Si_{1-x}Ge_x$ Contacts for VLSI Applications," *Electronics Letters*, 2000, 36(21):1819–1821.

Ponomarev et al., "High–Performance Deep SubMicron CMOS Technologies with Polycrystalline–SiGe Gates," *IEEE Transactions on Electron Devices*, vol. 47, No. 4, Apr. 2000, pp. 848–855.

Yasuda et al., "Interfacial Reactions of Ti/ and Zr/$Si_{1-x}Ge_x$/Si Contacts with Rapid Thermal Annealing," *Thin Solid Films*, 2000, 373:73–78.

Gannavaram, et al., "Low Temperature (≦800° C.) Recessed Junction Selective Silicon–Germanium Source/Drain Technology for sub–70 nm CMOS," *IEEE International Electron Device Meeting Technical Digest*, (2000), pp. 437–440.

Ge et al., "Process–Strained Si (PSS) CMOS Technology Featuring 3D Strain Engineering," *IEEE International Electron Devices Meeting Technical Digest*, (2003) pp. 73–76.

Ghani et al., "A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors," *IEEE International Electron Devices Meeting Technical Digest*, (2003), 978–980.

Hamada et al., "A New Aspect of Mechanical Stress Effects in Scaled MOS Devices," *IEEE Transactions on Electron Devices*, vol. 38, No. 4 (Apr. 1991), pp. 895–900.

Huang et al., "Isolation Process Dependence of Channel Mobility in Thin–Film SOI Devices," *IEEE Electron Device Letters*, vol. 17, No. 6 (Jun. 1996), pp. 291–293.

Huang et al., "LOCOS–Induced Stress Effects on Thin–Film SOI Devices," *IEEE Transactions on Electron Devices*, vol. 44, No. 4 (Apr. 1997), pp. 646–650.

Huang, et al., "Reduction of Source/Drain Series Resistance and Its Impact on Device Performance for PMOS Transistors with Raised $Si_{1-x}Ge_x$ Source/Drain", *IEEE Electron Device Letters*, vol. 21, No. 9, (Sep. 2000) pp. 448–450.

Iida et al., "Thermal behavior of residual strain in silicon–on–insulator bonded wafer and effects on electron mobility," *Solid–State Electronics*, vol. 43 (1999), pp. 1117–1120.

Ito et al., "Mechanical Stress Effect on Etch–Stop Nitride and its Impact on Deep Submicron Transistor Design," *IEEE International Electron Devices Meeting Technical Digest*, (2000), pp. 247–250.

Lochtefeld et al., "Investigating the Relationship Between Electron Mobility and Velocity in Deeply Scaled NMOS via Mechanical Stress," *IEEE Electron Device Letters*, vol. 22, No. 12 (2001), pp. 591–593.

Ootsuka et al., "A Highly Dense, High–Performance 130nm node CMOS Technology for Large Scale System–on–a–Chip Applications," *IEEE International Electron Devices Meeting Technical Digest*, (2000), pp. 575–578.

Ota et al., "Novel Locally Strained Channel Technique for High Performance 55nm CMOS," *IEEE International Electron Devices Meeting Technical Digest*, (2002), pp. 27–30.

Öztürk, et al., "Advanced $Si_{1-x}Ge_x$ Source/Drain and Contact Technologies for Sub–70 nm CMOS," *IEEE International Electron Device Meeting Technical Digest*, (2002), pp. 375–378.

Öztürk, et al., "Low Resistivity Nickel Germanosilicide Contacts to Ultra–Shallow $Si_{1-x}Ge_x$ Source/Drain Junctions for Nanoscale CMOS," *IEEE International Electron Device Meeting Technical Digest* (2003), pp. 497–500.

Öztürk, et al., "Selective Silicon–Gremanium Source/Drain Technology for Nanoscale CMOS," *Mat. Res. Soc. Symp. Proc.*, vol. 717, (2002), pp. C4.1.1–C4.1.12.

Öztürk, et al., "Ultra–Shallow Source/Drain Junctions for Nanoscale CMOS Using Selective Silicon–Germanium Technology," *Extended Abstracts of International Workshop on Junction Technology*, (2001), pp. 77–82.

Shimizu et al., "Local Mechanical–Stress Control (LMC): A New Technique for CMOS–Performance Enhancement," *IEEE International Electron Devices Meeting Technical Digest*, (2001), pp. 433–436.

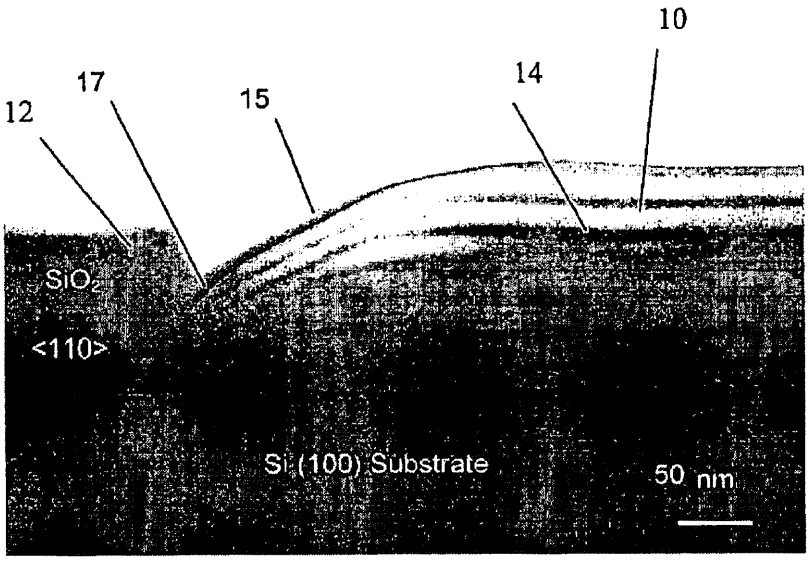
Thompson et al., "A Logic Nanotechnology Featuring Strained–Silicon," *IEEE Electron Device Letters*, vol. 25, No. 4 (Apr. 2004), pp. 191–193.

Thompson et al., "A 90 nm Logic Technology Featuring 50nm Strained–Silicon Channel Transistors, 7 layers of Cu *Interconnects*, Low k ILD, and $1um^2$ SRAM Cell," *IEEE International Electron Devices Meeting Technical Digest*, (2002), pp. 61–64.

Tiwari et al., "Hole Mobility Improvement in Silicon–on–Insulator and Bulk Silicon Transistors Using Local Strain," *IEEE International Electron Devices Meeting Technical Digest*, (1997), pp. 939–941.

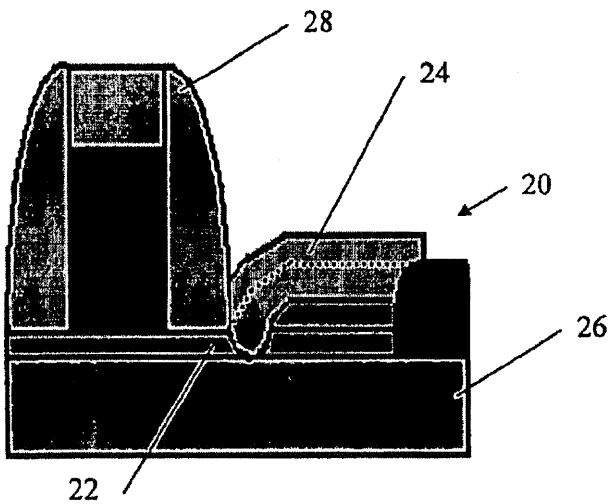
Uchino, et al., "A Raised Source/Drain Technology Using In–situ P–doped SiGe and B–doped Si for 0.1–μm CMOS ULSIs," *IEEE International Electron Device Meeting Technical Digest*, (1997), pp. 479–482.

* cited by examiner



Prior Art

FIG. 1



Prior Art

FIG. 2

Prior Art

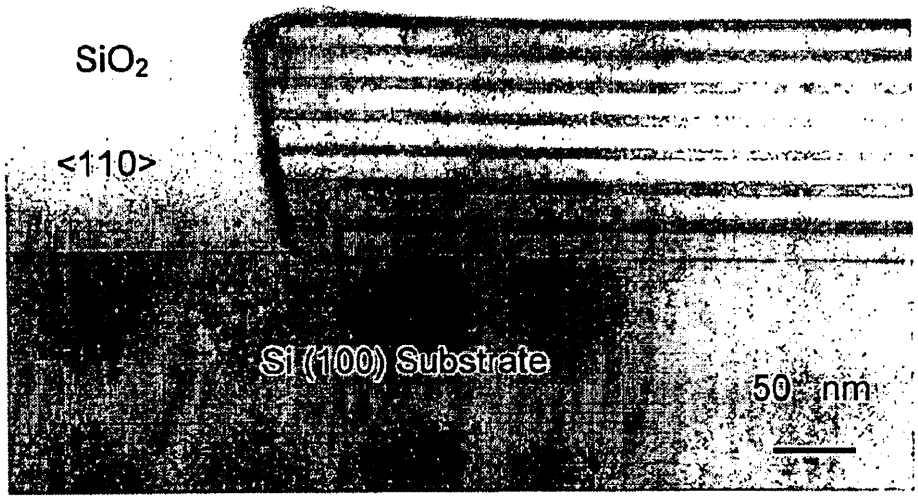


FIG. 3

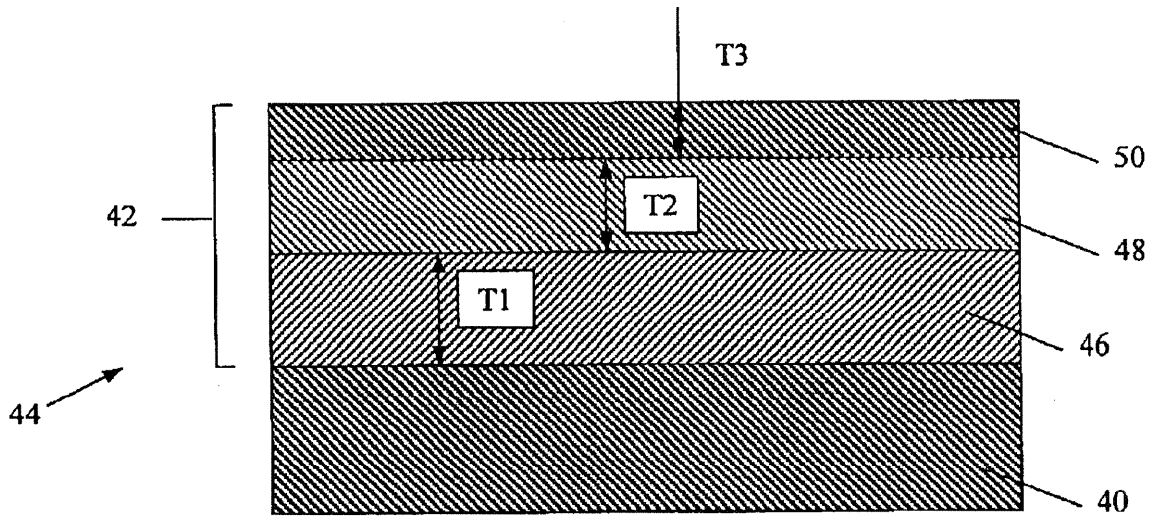


FIG. 4

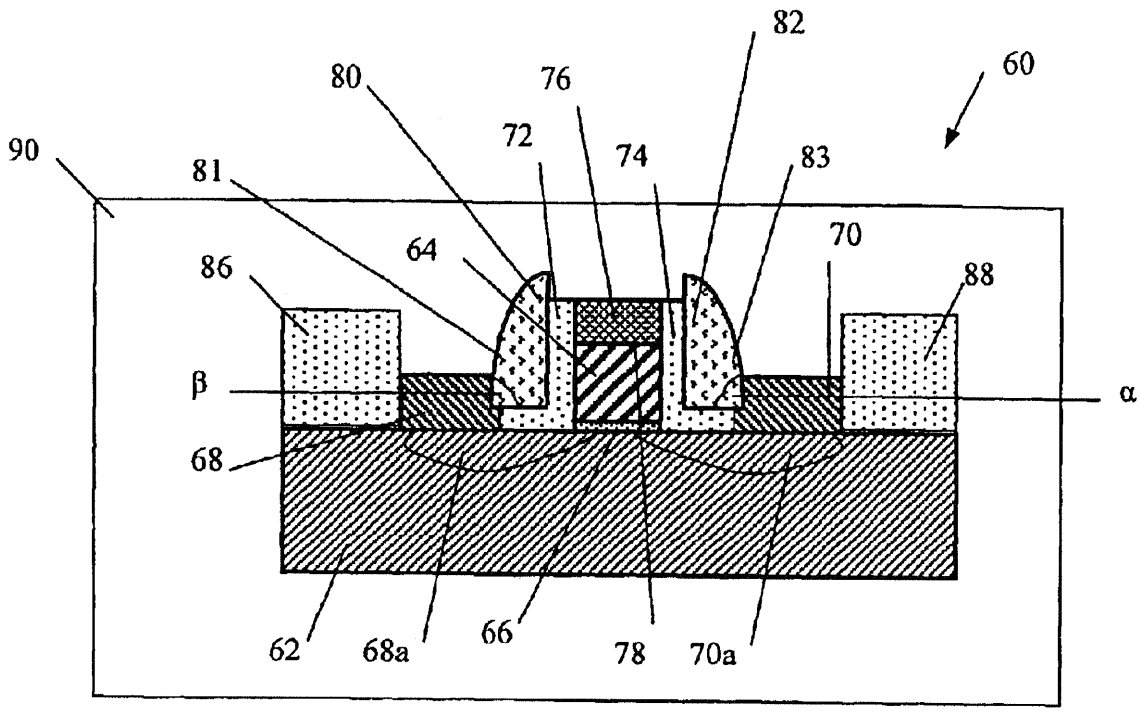


FIG. 5

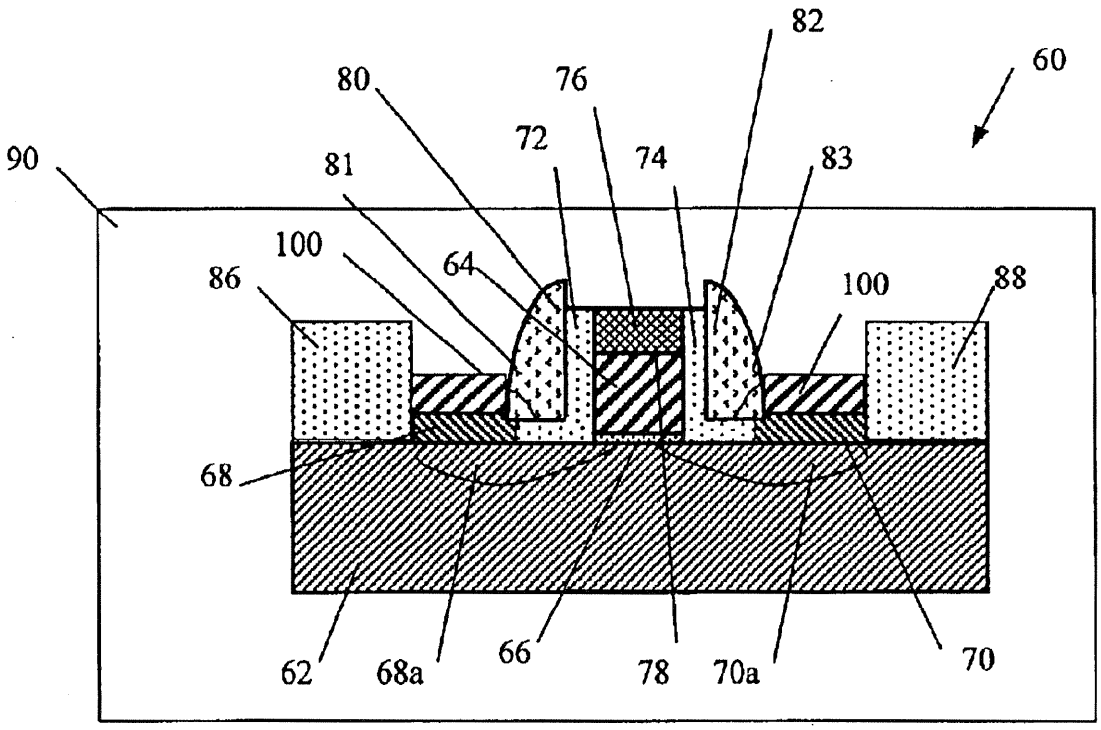


FIG. 6

METHODS OF FABRICATING SEMICONDUCTOR STRUCTURES HAVING EPITAXIALLY GROWN SOURCE AND DRAIN ELEMENTS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority to and the benefit of U.S. Provisional Application Ser. No. 60/387,867 filed Jun. 10, 2002, the entire disclosure of which is incorporated herein by reference.

FIELD OF THE INVENTION

The present invention relates generally to semiconductor fabrication methods and, more specifically, to methods for fabricating semiconductor devices having substantially facetless raised source and drain elements.

BACKGROUND

In order to improve performance and packing density of modern microelectronic devices, it is often desirable to reduce channel lengths of metal-oxide-semiconductor-field-effect transistors ("MOSFETs") during device design. As the MOSFET channel length decreases, however, short channel effects and parasitic resistance become of increasing concern. To minimize short channel effects in bulk silicon devices, for example, the source/drain doping junction depths are decreased during scaling. But shallower junctions require the use of thinner silicides to minimize leakage current from the silicon/silicide interface to the junction depletion region, which, at the same time, may increase parasitic contact resistances. As another example, to improve performance of a silicon-on-insulator ("SOI") device by reducing short channel effects, its silicon region should preferably be less than about 20 nm thick. Conventional silicide formation processes, however, may consume substantially the entire silicon layer of such thickness, which may, in turn, result in undesirably large leakage currents and parasitic contact resistance because the silicide/silicon interface area is small.

The increasing operating speeds and computing power of microelectronic devices have recently given rise to the need for an increase in the complexity and functionality of the semiconductor substrates that are used as the starting substrate in these microelectronic devices. Such "virtual substrates" based on silicon and germanium provide a platform for new generations of VLSI devices that exhibit enhanced performance when compared to devices fabricated on bulk Si substrates. Specifically, new technological advances enable formation of heterostructures using silicon-germanium alloys (hereinafter referred to as "SiGe" or "$Si_{1-x}Ge_x$") to further increase performance of the semiconductor devices by changing the atomic structure of Si to increase electron mobility. These substrates are called strained Si substrates.

A strained Si substrate is generally formed by a first epitaxial growth of a relaxed SiGe layer on bulk Si, and then a second epitaxial growth of a thin (less than about 500 Å) Si layer on the relaxed SiGe layer. Because the lattice constant of relaxed SiGe heterostructure is different from Si, the thin Si layer becomes "strained," resulting in enhanced mobilities (and hence improved device speeds) over bulk Si. The percentage of Ge in SiGe, and the method of deposition can have a dramatic effect on the characteristics of the strained Si layer. U.S. Pat. No. 5,442,205, "Semiconductor

Heterostructure Devices with Strained Semiconductor Layers," incorporated herein by reference, demonstrates one such method of producing a strained Si device structure.

A method of epitaxially growing a relaxed SiGe layer on bulk Si is discussed in international application WO 01/22482, "Method of Producing Relaxed Silicon Germanium Layers," incorporated herein by reference. The method includes providing a monocrystalline Si substrate, and then epitaxially growing a graded $Si_{1-x}Ge_x$ layer with increasing Ge concentration at a gradient of less than 25% Ge per micron to a final composition in the range of $0.1 < x < 1$, using a source gas of $Ge_xH_yCl_z$ for the Ge component, on the Si substrate at a temperature in excess of 850° C. and then epitaxially growing a semiconductor material on the graded layer.

Another method of epitaxially growing a relaxed SiGe layer on bulk Si is discussed in a paper entitled, "Low Energy plasma enhanced chemical vapor deposition," by M. Kummer et. al. (Mat. Sci. & Eng. B89, 2002, pp. 288–95), incorporated herein by reference, in which a method of low-energy plasma-enhanced chemical vapor deposition (LEPECVD) is shown, which allows the formation of a SiGe layer on bulk Si at high growth rates (0.6 micron per minute) and low temperatures (500–750° C.).

To grow a high-quality, thin, epitaxial strained Si layer on a graded SiGe layer, the SiGe layer is, preferably, planarized to reduce the surface roughness in the final strained Si substrate. Current methods of chemical mechanical polishing (CMP) are typically used to improve the planarity of surfaces in semiconductor fabrication processes. U.S. Pat. No. 6,107,653, "Controlling Threading Dislocations in Ge on Si Using Graded GeSi Layers and Planarization," incorporated herein by reference, describes how planarization can be used to improve the quality of SiGe graded layers.

Although the resulting biaxial tensile or compressive strain alters the carrier mobilities in the layers of the "virtual substrate" enabling the fabrication of high-speed and/or low-power devices, short channel effects and parasitic resistance remain of concern for strained-Si-based devices as well.

Raised source/drain structures have been proposed as a technique for forming high-quality contacts to improve performance of bulk silicon, silicon-on-insulator (SOI), and strained silicon devices. Raised source/drains are generally fabricated by raising the level of the source and drain regions by selective semiconductor, e.g., silicon, deposition. The extra silicon increases the process margin for the silicide process and extends the latitude for contact junction design. To maintain a similar crystalline structure, the extra silicon is "grown" by silicon epitaxy.

For example, in bulk and strained Si devices, raised source/drain contacts have been proposed as a means of forming shallow dopant junctions to minimize contact resistances and short channel effects. In SOI devices, the raised source and drain regions provide sacrificial silicon useful for silicide consumption to form low resistance contacts on thin Si films.

Typically, source and drain regions are formed by selective epitaxial silicon growth after formation of a sidewall dielectric spacer of silicon dioxide (SiO_2), silicon nitride (Si_3N_4), or a combination of both materials. In this process, silicon is epitaxially grown on exposed windows in a dielectric mask while nucleation of polysilicon on the masking material is suppressed during the incubation time by, for example, etching of spurious nuclei on the dielectric material by hydrogen chloride, the mediation of saturation by

formation of a number of intermediate chlorine-containing silicon precursors, and passivation of surface defect sites which serve as heterogeneous nucleation centers. Also, selectivity is facilitated by growing for a period of time that is generally shorter than the incubation period needed for polysilicon nucleation on the dielectric mask.

The dielectric spacer electrically isolates a gate made of, for example, polysilicon, from the source and drain regions. After the selective epitaxial growth step, a heavy low-energy implant forms a doped region, and is followed by a silicidation process for, e.g., low resistance complementary metal-oxide-semiconductor (CMOS) contacts.

During selective epitaxial growth, however, decreased thickness of the epitaxial layer typically occurs at interfaces between the epitaxial layer and the dielectric spacer or field oxide, where facets form by growth of low-energy crystal planes that minimize the energetically less favorable epitaxial Si/dielectric material interface. Because the raised source/drain regions grow thinner near the dielectric spacer edge, faceting leads to non-planar device layers. This phenomenon raises processing concerns in bulk Si, SOI, and strained Si devices by complicating implementation of selective epitaxial growth in device applications. Specifically, thinner faceted regions cause localized deeper dopant penetration during ion implantation, which increases short channel effects and leakage currents. Also, thinner faceted regions typically result in deeper silicide penetration and greater Si consumption during silicidation. Thus, faceting may result in poor doping profile control and poor silicide depth control, leading to degraded device characteristics and more complex device designs.

For example, referring to FIG. **1**, a cross-sectional transmission electron microscope (XTEM) image illustrates undoped Si layers **10** grown adjacent to reactive ion etched <110>-oriented SiO_2 sidewalls **12**. The SiGe layers **14** were included as markers to track facet development and evolution. The selective Si epitaxy has noticeable (311)-oriented facets **15** and (110)-oriented facets **17** next to Sio_2 sidewalls. Such faceting would be detrimental during implant and silicidation of source and drain regions. Referring to FIG. **2**, a silicided source region **20** is formed by selective epitaxial growth on a thin film SOI substrate **22** according to any method known in the art. Such faceted growth leads to deep penetration of a silicide **24** to a buried SiO_2 layer **26**. This penetration may dramatically increase the contact resistance because the silicide/silicon channel interfacial area is reduced, which leads to poor device characteristics. The electrical contact to the device channel is made through the area adjacent to the spacer **28**, which is only the width of the Si channel. Furthermore, the contact quality may degrade because of incomplete silicide formation if the thickness of consumed Si is insufficient.

Similarly, in strained-Si-based devices, thinner faceted raised source and drain regions may cause the silicide to penetrate into a relaxed silicon-germanium (SiGe) layer underneath a strained Si layer. This may result in formation of a poor quality silicide because of the rejection of Ge during alloying of the SiGe layer with the silicide metal. This rejection may create high-resistivity regions that compromise the contact quality.

Facetless selective epitaxial growth is, therefore, desirable for fully realizing the performance advantages of the raised source/drain scheme for fabrication of low-resistance contacts and shallow junctions in advanced devices that have wide ranging application to Si, SOI, and strained Si technologies.

Recently, facetless epitaxy has received much attention in the design of raised source/drain contacts for CMOS applications. For example, selective growth in inverse patterns, i.e. using Sio_2 pillars with a Si field as opposed to Si windows in a SiO_2 field, has been proposed. Another approach involves fabrication of facetless raised source/drain structures by selective epitaxial growth in commercially available low-pressure and atmospheric-pressure chemical vapor deposition systems by carefully controlling the geometry of the multilayer spacer structure and sidewall spacer profile. For example, it has been suggested that undercutting the liner oxide and silicon growth under the silicon nitride spacer recesses the silicon-liner oxide interaction away from the source/drain region. This gives extra thickness in the source/drain region before the increase in silicon-dielectric interface energy causes the epitaxial layer to facet.

In yet another approach, discussed in a thesis entitled "Selective SiGe Nanostructures" by Tom Langdo (Ph.D. Thesis, MIT, 2001)("Langdo thesis"), incorporated herein by reference, facetless growth was demonstrated by in situ n-type doping of a silicon layer being deposited by selective epitaxy adjacent to a sidewall of a reactive ion etched SiO_2 spacer in a ultra-high vacuum chemical vapor deposition (UHVCVD) system. It was demonstrated that a combination of moderate n-type doping and relatively vertical SiO_2 sidewalls results in facet-free epitaxy along <110>-oriented SiO_2 sidewalls. Referring to FIG. **3**, an XTEM image illustrates growth of 1×10^{18} /cm^3 n-type doped Si with $Si_{0.9}Ge_{0.1}$ marker layers on <110>-oriented SiO_2 sidewalls. As shown in FIG. **3**, all $Si_{0.9}Ge_{0.1}$ marker layers follow (100) planes, and thus, facet formation is suppressed during the growth. SiO_2 was chosen as the sidewall material instead of more commonly used Si_3N_4 because selective growth generally cannot be achieved with either SiH_4 or SiH_2Cl_2 source gases, common Si precursors, on Si_3N_4 spacers without the addition of hydrogen chloride. Because of the deleterious effects of chloride on a UHVCVD system, however, addition of hydrogen chloride to the source gases is impractical.

Obstacles hinder the commercialization of this UHVCVD growth approach. First, UHVCVD is generally not feasible for large-scale commercial applications. Second, UHVCVD selective growth is not possible with Si_3N_4 dielectric materials. Finally, the UHVCVD process described above is generally not compatible with multi-layered commercial spacer structures that include, e.g., Si_3N_4 materials.

Thus, there remains a need in the art for a process of fabricating semiconductor devices having facetless raised source/drain structures that is compatible with existing semiconductor manufacturing processes, systems, and materials and that also possesses improved process tolerances.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a process for fabricating facetless semiconductor structures that overcomes the limitations of known processes. Specifically, it is an object of the invention to provide a process for fabricating semiconductor devices having facetless raised source/drain structures that complements existing epitaxial processes and does not require stringent control of the geometry of the dielectric regions. It is also desirable that such process be less expensive in comparison to the manufacturing processes known in the art and not limited to a particular dielectric or semiconductor material.

Accordingly, methods for fabricating facetless semiconductor structures using commercially available chemical

vapor deposition systems are disclosed herein. A key aspect of the invention includes selectively depositing an epitaxial layer of at least one semiconductor material on the semiconductor substrate while in situ doping the epitaxial layer to suppress facet formation. Suppression of facet formation during selective epitaxial growth by in situ doping of the epitaxial layer at a predetermined level rather than by manipulating spacer composition and geometry alleviates the stringent requirements on the device design. For example, in various embodiments of the fabrication methods according to the invention, it is not necessary to precisely control the liner oxide undercut beneath the silicon nitride spacer prior to epitaxial growth to minimize faceting, thus making the process more robust and compatible with very thin spacer dimensions. Accordingly, in situ doping during epitaxial growth to suppress faceting increases tolerance to variability during the spacer fabrication, providing an improved robust process suitable for volume manufacturing.

Throughout the following description, the term "facet" is used to refer generally to a slanted low-energy crystal plane formed in a semiconductor material at its interface with a dielectric material. Further, the term "epitaxy" is used to refer generally to methods for growing thin layers of single crystal materials on a single crystal substrate whereby crystallographic structure of the substrate is reproduced in the deposited material. Also, the term "MOS" is used to refer generally to semiconductor devices that include a conductive gate spaced at least by an insulating layer from a semiconducting channel layer. Conversely, the terms "MOSFET" or "MOS transistor" refer to a field-effect transistor having a conductive gate spaced at least by an insulating layer from a semiconducting channel layer. The terms "SiGe" and "$Si_{1-x}Ge_x$" are used interchangeably to refer to silicon-germanium alloys. The term "silicide" is here used to refer to a reaction product of a metal, silicon, and optionally other components, such as germanium. The term "silicide" is also used, less formally, to refer to the reaction product of a metal with an elemental semiconductor, a compound semiconductor or an alloy semiconductor. The term "doping" is used to refer generally to the process of adding impurities to a semiconductor material to achieve desired properties.

In general, in one aspect, the invention is directed to a method of fabricating a semiconductor structure including the steps of providing a chamber and providing a semiconductor substrate in the chamber. The semiconductor substrate has a surface including a first portion and a second portion proximal to the first portion. The method of the invention also includes forming a dielectric region on the first portion of the substrate and selectively depositing an epitaxial layer of at least one semiconductor material on the second portion of the substrate while in situ doping the epitaxial layer. The in situ doping occurs at a first predetermined level to substantially suppress facet formation thereby forming a substantially facetless semiconductor region. The pressure in the chamber during selective deposition of the epitaxial layer is greater than about 5 Torr.

In one embodiment of the invention, the epitaxial layer is deposited in a chemical vapor deposition system, such as, for example, a reduced-pressure chemical vapor deposition system, atmospheric-pressure chemical vapor deposition system, or plasma-enhanced chemical vapor deposition system.

In another embodiment of the invention, the step of selectively depositing an epitaxial layer includes introducing a source gas into the chamber. The source gas may include at least one precursor gas and a carrier gas, such as, for example hydrogen. According to one feature of this embodiment, the at least one precursor gas includes a silicon precursor gas, such as, for example, silane, disilane, trisilane, or dichlorosilane. According to another feature of this embodiment, the at least one precursor gas includes a germanium precursor gas, such as, for example, germane, digermane, germanium tetrachloride, or germanium dichloride. According to yet another feature of this embodiment, in addition to the at least one precursor gas and a carrier gas, the source gas also includes an etchant for suppressing nucleation of the at least one semiconductor material over the dielectric region during deposition. The etchant may include hydrogen chloride or chlorine.

In yet another embodiment of the invention, the epitaxial layer is doped by adding a dopant to the epitaxial layer during deposition of the epitaxial layer. Examples of suitable dopants are phosphorus, arsenic, antimony, and boron. The dopant may be added to the epitaxial layer by introducing a dopant gas, such as phosphine, arsine, stibine, and diborane, into the chamber. According to one feature of this embodiment, the first predetermined level of doping ranges from about 10^{17} to about 10^{19} cm^{-3}

The epitaxial layer may include at least one of silicon and germanium. Also, the dielectric region may include at least one of silicon oxide and silicon nitride. Optionally, the dielectric region may have a two-layered spacer structure including a silicon oxide layer and a silicon nitride layer disposed thereon.

In some embodiments of the invention, the semiconductor substrate includes silicon. In other embodiments, the semiconductor substrate may include a silicon wafer; an insulating layer disposed thereon; and a strained semiconductor layer, for example, silicon or germanium, disposed on the insulating layer. Alternatively, the semiconductor substrate may include a silicon wafer; a compositionally uniform relaxed $Si_{1-x}Ge_x$ layer deposited thereon; and a strained silicon layer deposited on the relaxed $Si_{1-x}Ge_x$ layer. In this embodiment, the semiconductor substrate may also include a compositionally graded $Si_{1-x}Ge_x$ layer disposed between the compositionally uniform relaxed $Si_{1-x}Ge_x$ layer and the silicon wafer, or an insulating layer disposed between the compositionally uniform relaxed $Si_{1-x}Ge_x$ layer and the silicon wafer.

In still another embodiment of the invention, the temperature in the chamber during selective deposition of the epitaxial layer ranges from about 300° C. to about 900° C., for example, from about 500° C. to about 700° C. Also, the epitaxial layer may be deposited at a rate greater than about 1 nm/min.

In one embodiment of the invention, the method includes the steps of fabricating an n-channel MOSFET in a first portion of the semiconductor region; and fabricating a p-channel MOSFET in a second portion of the semiconductor region. According to one feature of this embodiment, the method includes counter-doping the first portion or the second portion at a second predetermined level. Optionally, the first predetermined level of doping does not exceed the second predetermined level of doping.

In some embodiments, the method of the invention also includes forming a metal silicide layer over the semiconductor region. The surface of the semiconductor substrate may have a substantially (100) crystallographic orientation. Also, the dielectric region may include a sidewall having an angle relative to the semiconductor substrate that ranges from about 60° to about 90°. The sidewall may be substantially aligned with either the <110> crystallographic plane or the <100> crystallographic plane of the semiconductor substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings, like reference characters generally refer to the same parts throughout the different views. Also, the drawings are not necessarily to scale, emphasis instead generally being placed upon illustrating the principles of the invention. In the following description, various embodiments of the present invention are described with reference to the following drawings, in which:

FIG. **1** depicts an XTEM image illustrating faceted selective epitaxial growth of alternating Si and SiGe layers proximate a sidewall of a SiO_2 spacer according to methods known in the art

FIG. **2** depicts a cross-sectional schematic view of a semiconductor device having a faceted raised source region according to methods known in the art;

FIG. **3** depicts an XTEM image illustrating facetless selective epitaxial growth according to one method known in the art;

FIG. **4** depicts a cross-sectional view of a semiconductor substrate suitable for use with various embodiments of the invention;

FIG. **5** depicts a cross-sectional view of a semiconductor device having selectively grown and in situ doped facetless Si source/drain epitaxial layers according to the invention; and

FIG. **6** depicts a cross-sectional view of the device of FIG. **5** after silicidation of the source/drain epitaxial layers.

DETAILED DESCRIPTION

In various embodiments of the invention, facetless semiconductor structures, for example, raised source and drain elements of a MOSFET, are fabricated by selective epitaxial growth proximate commonly used spacer structures, such as those including Si_3N_4, SiO_2, or both, using commercially available chemical vapor deposition systems. Facet formation in the epitaxial layer is suppressed by doping the epitaxial layer at a predetermined level in situ during epitaxial growth, which increases tolerance to variability during the spacer fabrication process.

Referring to FIG. **4**, a substrate **40** suitable for use with the invention, comprises a semiconductor, such as silicon or silicon deposited over an insulator, such as, for example, SiO_2. In one embodiment, several layers collectively indicated as **42** are formed on the substrate **40**. The layers **42** may be grown, for example, in a CVD system, including a reduced-pressure chemical vapor deposition system (LPCVD), atmospheric-pressure chemical vapor deposition system (APCVD), and plasma-enhanced chemical vapor deposition system (PECVD). In this embodiment, the layers **42** and the substrate **40** may be referred to together as a "semiconductor substrate **44**."

The layers **42** include a graded layer **46** disposed over the substrate **40**. The graded layer **46** may include SiGe with a grading rate of, for example, 10% Ge/μm of thickness, with a thickness T1 of, for example, 2–9 μm, and grown, for example, at 600–1100° C. A relaxed layer **48** is disposed over the graded layer **46**. The relaxed layer **48** may include, for example, $Si_{1-x}Ge_x$ with a uniform composition containing, for example, 20–90% Ge, (i.e., $0.2 \leqq x \leqq 0.9$) having a thickness T2 ranging from, e.g., about 0.2 μm to about 2 μm. In an alternative embodiment, the relaxed layer **48** may be formed directly on the substrate **40**, without the graded layer **46**.

A tensilely strained layer **50** is disposed over relaxed layer **48**, sharing an interface therewith. In one embodiment, the tensilely strained layer **50** is formed of silicon. In other embodiments, the tensilely strained layer **50** may be formed of SiGe, or at least one of a group II, a group III, a group V, and a group VI element. The tensilely strained layer **50** may have a starting thickness T3 ranging, for example, from about 50 angstroms to about 300 angstroms (Å).

In some embodiments, a compressively strained layer (not shown) may be disposed between the relaxed layer **48** and the tensilely strained layer **50**. In an embodiment, the compressively strained layer includes $Si_{1-y}Ge_y$ with a Ge content (y) higher than the Ge content (x) of the relaxed $Si_{1-x}Ge_x$ layer **48**. The compressively strained layer may contain, for example 40–100% Ge and have a thickness ranging, e.g., from about 10 angstroms to about 200 angstroms (Å).

Referring to FIG. **5**, in one embodiment, a semiconductor device, such as, for example, a transistor **60** having facetless raised source/drain regions is fabricated in a chamber **90** of a chemical vapor deposition system, such as, for example, LPCVD, APCVD, or PECVD system. The transistor **60** is formed on a semiconductor substrate **62** including, for example, silicon, silicon-on-insulator, or strained silicon, as described in detail above. The surface of the semiconductor substrate may have a substantially (100) crystallographic orientation.

In a particular variation of this embodiment of the invention, prior to MOSFET fabrication, the substrate **62** is cleaned using, for example, a dilute RCA process known in the art, in order to remove organic contaminants, particles, and any ionic or heavy metal contaminants from the substrate surface. Alternatively, or in addition to the RCA cleaning, the surface of the substrate may be passivated with hydrogen using a dilute hydrofluoric acid treatment. In yet another variation, a sacrificial SiO_2 layer may be grown on the substrate thermally or by an oxygen plasma and then completely removed by hydrofluoric acid. In still another variation, a non-selective dry-etch process can be used. The clean surface must be achieved while minimizing substrate consumption to ensure compatibility with thin film materials heterostructures and SOI wafers. Prior to epitaxial growth the substrate may be subjected to a high temperature bake step to remove any residual oxide on the surface. For example, after hydrogen passivation with a dilute HF treatment a suitable bake could include heating the substrate for 5 minutes at 800° C.

The transistor 60 includes a gate electrode **64**, made of, for example, polycrystalline silicon, and a gate insulator **66** made of, for example, SiO_2 or a high-k material, patterned using, for example, reactive ion etching ("RIE") whereby SiO_2 gate insulator is defined by selective reactive ion etching using, e.g. CHF_3 /O_2 gas mixture with subsequent post-RIE cleaning to remove the growth-inhibiting fluoropolymer layer, as described in the above-referenced Langdo thesis.

Isolation regions **86**, **88**, made of, e.g., SiO_2, are introduced to isolate transistor **60** from other devices. Isolation regions **86**,**88** can be, for example, shallow trench isolation regions produced early in the transistor fabrication process by methods known in the art.

The transistor **60** also includes a source region **68** and a drain region **70** defined in the substrate **60** proximate the gate electrode **64**. In a particular embodiment, the transistor **60** is an n-type MOSFET with the source and drain regions formed by n-type doping via, e.g. implantation of arsenic ions, as will be described in detail below. Shallow extension regions **68***a*, **70***a* of the source region **68** and the drain region

70, respectively, are formed by, e.g., ion implantation after the gate electrode **64** and the gate insulator **66** are defined. The shallow extension regions **68***a*, **70***a* preferably extend to and, in one variation of this embodiment, slightly below the gate insulator **66**. The depth of the extension regions **68***a*, **70***a* may range from about 5 nm to about 50 nm. A first liner **72** and a second liner **74** are deposited proximate the gate electrode **64** and the gate insulator **66**. In a particular embodiment, the thickness of the liners **72**, **74** is approximately 250 angstroms. The liners **72**, **74** may be formed of, e.g., a low temperature oxide (LTO). During the formation of liners **72**, **74**, a hard mask **76** is formed on a top surface **78** of the gate electrode **64**. Hard mask **76** is formed of, e.g., LTO.

Subsequently, spacers **80**, **82** are formed proximate liners **72**, **74** to electrically isolate the gate and source/drain regions during the device operation. The spacers **80**, **82** are formed of a dielectric such as, for example, Si_3N_4, by chemical vapor deposition followed by an etchback step, such as reactive ion etch. Alternatively, spacers can be formed from SiO_2. In one embodiment, the height of the spacers **80**, **82** roughly approximates or exceeds the height of the gate electrode **64** and ranges from about 80 nm to about 250 nm. The widths of the spacers **80**, **82** range from about 30 nm to about 100 nm. Spacer sidewalls **81**, **83** proximate to the source/drain regions **68**, **70** may have at least partially concave profile. Sidewalls **81**, **83** intersect the surface of the substrate **62** at angles α, β that range from about 60° to about 90°. In a particular embodiment, the angles α, β substantially, but not necessarily precisely, equal 90°. Furthermore, in various embodiments of the fabrication methods according to the invention, it is not necessary to precisely control the liner oxide undercut beneath the silicon nitride spacer prior to epitaxial growth to minimize faceting. The spacers **80**, **82** may be fabricated so that the sidewalls **81**, **83** are substantially aligned with a particular crystallographic plane of the semiconductor substrate **62**, such as, for example, the <100> or <110> crystallographic plane.

The raised source/drain regions **68**, **70** are formed by selective epitaxial growth coupled with ion implantation after formation of sidewall spacers **80**, **82**, as described below. The height of the source/drain regions **68**, **70** may range from about 10 nm to about 100 nm.

Referring to FIG. **6**, a contact material **100** is subsequently formed on raised source and drain regions **68**, **70**. In a particular embodiment, the contact material **100** is a metal compound that is thermally stable and has low electrical resistivity at the silicon/refractory metal interface, such as a metal silicide including, for example, cobalt, titanium, tungsten, molybdenum, platinum, nickel, or tantalum. Preferably, the contact material **90** is formed by a self-aligned silicide process, in which the contacts are formed only in the areas where the deposited metal is in direct contact with the source/drain regions **68**, **70**. Because of the facet-free formation, the metal uniformly penetrates the raised source **68** and drain **70** regions thereby maintaining the advantages of the raised source and drain approach.

In various embodiments of the invention, the raised source/drain elements **68**, **70** include, for example, Si, Ge, or SiGe alloys, and are formed by selective epitaxial growth in a CVD system, such as LPCVD, APCVD, or PECVD reactor. Suitable CVD systems commonly used for volume epitaxy in manufacturing applications include, for example, EPI CENTURA™ single-wafer multi-chamber systems available from Applied Materials of Santa Clara, Calif., or EPSILON® single-wafer epitaxial reactors available from ASM International based in Bilthoven, The Netherlands.

In the CVD process, selective epitaxial growth typically includes introducing a source gas into the chamber. The source gas may include at least one precursor gas and a carrier gas, such as, for example hydrogen. In those embodiments of the invention where the raised regions **68**, **70** are formed from Si, silicon precursor gases such as, for example, silane, disilane, trisilane, or dichlorosilane (DCS) are used. Conversely, in those embodiments of the invention where the raised regions **68**, **70** are formed from Ge, germanium precursor gases, such as, for example, germane (GeH_4), digermane, germanium tetrachloride, or germanium dichloride are used. Finally, in the embodiments where the raised regions **68**, **70** are formed from SiGe alloy, a combination of silicon and germanium precursor gases in various proportions is used. In a particular embodiment of the invention for selective deposition of $Si_{0.80}$ $Ge_{0.20}$ layers, 100 standard cubic centimeters (sccm) of DCS, 25 sccm 10% GeH_4/H_2, and 150 sccm of HCl in a hydrogen carrier gas at a growth temperature of 750° C. and pressure of 20 Torr may be used. In another embodiment of the invention for selective deposition of Si layers, 100 sccm of DCS and 100 sccm of HCl in a hydrogen carrier gas at a growth temperature of 850° C. and pressure of 10 Torr may be used.

The LPCVD, APCVD, or PECVD system chamber is heated, such as, for example, by RF-heating. The growth temperature in the chamber ranges from about 300° C to about 900° C depending on the composition of the raised regions **68**, **70**. Specifically, if the source gas predominantly contains silicon precursor, the temperature preferably ranges from about 500 to about 900° C, and if the source gas predominantly contains germanium precursor, the temperature ranges from about 300° C to about 700° C. The chamber pressure during formation of raised regions **68**, **70** is greater than about 5 Torr and the growth rate is greater than 1 nanometer/minute (nm/min).

Referring again to FIG. **5**, during selective epitaxial growth, the material composing raised regions **68**, **70** forms only on the semiconductor substrate, such as the silicon substrate **62**. The top surface **78** of gate electrode **64** is protected from epitaxial growth by the hard mask **76**. Alternatively, hard mask **76** is absent from top surface **78** of gate electrode **64**, and epitaxial growth additionally occurs on top surface **78**. Epitaxy parameters are chosen such that substantially no epitaxial layer is formed on sidewall spacers **80**, **82**, and, as described below, substantially no facets are formed at the interface between raised regions **68**, **70** and spacers **80**, **82**.

Selective growth of epitaxial layers substantially only on silicon or other semiconductors, and not on dielectrics such as silicon nitride or silicon dioxide, is facilitated by the introduction of an etchant, such as, for example, hydrogen chloride or chlorine, to the source gas mixture. Specifically, epitaxial layers are grown on exposed windows in a dielectric mask while nucleation of polysilicon on the masking material is suppressed during the incubation time by, for example, etching of spurious nuclei on the dielectric material, the mediation of saturation by formation of a number of intermediate chlorine-containing silicon precursors, and passivation of surface defect sites which serve as heterogeneous nucleation centers. Also, selectivity is facilitated by growing for a period of time that is generally shorter than the incubation period needed for polysilicon nucleation on the dielectric mask.

In various embodiments of the invention, the epitaxial layers of the source/drain regions **68**, **70** are doped in situ by adding a dopant during deposition of the epitaxial layer to suppress facet formation at the interface with the spacers **80**,

82. Examples of suitable dopants are n-type dopant such as phosphorus, arsenic, and antimony, or p-type dopant, such as boron. The dopant may be added to the epitaxial layer by introducing a dopant gas, such as phosphine, arsine, stibine, and diborane, into the chamber. The dopant gas is diluted in a carrier gas of the source gas mixture to, for example, approximately 1% concentration.

In a particular embodiment, facetless selective epitaxial growth according to the invention is compatible with CMOS fabrication. CMOS fabrication entails formation of a n-channel MOSFET ("NMOS") in a first portion of the semiconductor region; and a p-channel MOSFET ("PMOS") in a second portion of the semiconductor region so that both MOSFETs are disposed on the same substrate. Accordingly, in this embodiment, in situ doping that is used during the epitaxial growth to suppress facet formation is sufficiently low so that it will not interfere with introduction of additional dopants of opposite type ("counterdoping") that is necessary in order to manufacture both n-channel and p-channel MOSFETs on the same substrate. This counterdoping may be performed with suitable masking in place for either NMOS (if the in situ doping to suppress faceting was p-type) or PMOS (if the in situ doping to suppress faceting was n-type), thus allowing CMOS fabrication. Accordingly, in this embodiment of the invention, a level of in situ doping that is used during the epitaxial growth to suppress facet formation does not exceed the level of counterdoping (for example, ion implantation) that is necessary for CMOS fabrication. For example, in one variation of this embodiment, the level of in situ doping ranges from about 10^{17} to about 10^{19} cm^{-3}, which does not interfere with a typical doping level used during CMOS fabrication that usually exceeds about 10^{20} cm^{-3}.

Other embodiments incorporating the concepts disclosed herein may be used without departing from the spirit and scope of the invention. The described embodiments are to be considered in all respects as only illustrative and not restrictive. Therefore, it is intended that the scope of the invention be only limited by the following claims.

What is claimed is:

1. A method of fabricating a semiconductor structure, the method comprising:

providing a chamber;

providing a semiconductor substrate in the chamber, the semiconductor substrate having a surface including a first portion and a second portion proximal to the first portion;

providing agate stack disposed over the first portion of said substrate, the gate stack comprising a dielectric region; and

selectively depositing an epitaxial layer of at least one semiconductor material on the second portion of the substrate adjacent to the gate stack while in situ doping the epitaxial layer at a first predetermined level to substantially suppress facet formation thereby forming a substantially facetless semiconductor region, wherein the pressure in the chamber during selective deposition of the epitaxial layer is greater than about 5 Torr.

2. The method of claim 1 wherein the epitaxial layer is deposited in a chemical vapor deposition system.

3. The method of claim 2 wherein the chemical vapor deposition system is selected from the group consisting of: a reduced-pressure chemical vapor deposition system, atmospheric-pressure chemical vapor deposition system, and plasma-enhanced chemical vapor deposition system.

4. The method of claim 1 wherein the step of selectively depositing an epitaxial layer comprises introducing a source gas into the chamber.

5. The method of claim 4 wherein the source gas comprises at least one precursor gas and a carrier gas.

6. The method of claim 5 wherein the carrier gas comprises hydrogen.

7. The method of claim 5 wherein the at least one precursor gas comprises a silicon precursor gas.

8. The method of claim 7 wherein the silicon precursor gas is selected from the group consisting of: silane, disilane, trisilane, and dichlorosilane.

9. The method of claim 5 wherein the at least one precursor gas comprises a germanium precursor gas.

10. The method of claim 9 wherein the germanium precursor gas is selected from the group consisting of: germane, digermane, germanium tetrachloride, or germanium dichloride.

11. The method of claim 5 wherein the source gas further comprises an etchant for suppressing nucleation of the at least one semiconductor material over the dielectric region during deposition.

12. The method of claim 11 wherein the etchant comprises hydrogen chloride or chlorine.

13. The method of claim 1 wherein the epitaxial layer is doped by adding a dopant to the epitaxial layer during deposition of the epitaxial layer, the dopant selected from the group consisting of: phosphorus, arsenic, antimony, and boron.

14. The method of claim 13 wherein the dopant is added to the epitaxial layer by introducing a dopant gas into the chamber, the dopant gas selected from the group consisting of: phosphine, arsine, stibine, and diborane.

15. The method of claim 13 wherein the first predetermined level of doping ranges from about 10^{17} to about 10^{19} cm^{-3}.

16. The method of claim 1 wherein the epitaxial layer comprises at least one of silicon and germanium.

17. The method of claim 1 wherein the dielectric region comprises at least one of silicon oxide and silicon nitride.

18. The method of claim 17 wherein the dielectric region comprises a two-layered spacer structure comprising a silicon oxide layer and a silicon nitride layer disposed thereon.

19. The method of claim 1 wherein the semiconductor substrate comprises silicon.

20. The method of claim 1 wherein the semiconductor substrate comprises

a silicon wafer;

an insulating layer disposed thereon; and

a strained semiconductor layer disposed on the insulating layer.

21. The method of claim 20 wherein the strained semiconductor layer comprises silicon or germanium.

22. The method of claim 1 wherein the semiconductor substrate comprises

a silicon wafer;

a compositionally uniform relaxed $Si_{1-x}Ge_x$ layer deposited thereon; and

a strained silicon layer deposited on the relaxed $Si_{1-x}Ge_x$ layer.

23. The method of claim 22 wherein the semiconductor substrate further comprises a compositionally graded $Si_{1-x}Ge_x$ layer disposed between the compositionally uniform relaxed $Si_{1-x}Ge_x$ layer and the silicon wafer.

24. The method of claim 22 wherein the semiconductor substrate further comprises an insulating layer disposed between the compositionally uniform relaxed $Si_{1-x}Ge_x$ layer and the silicon wafer.

25. The method of claim 1 wherein the temperature in the chamber during selective deposition of the epitaxial layer ranges from about 300° C. to about 900° C.

26. The method of claim **25** wherein the temperature in the chamber during selective deposition of the epitaxial layer further ranges from about 500° C. to about 700° C.

27. The method of claim **1** wherein the epitaxial layer is deposited at a rate greater than about 1 nm/min.

28. The method of claim 1 further comprising:

fabricating a n-channel MOSFET in a first portion of the semiconductor region; and

fabricating a p-channel MOSFET in a second portion of the semiconductor region.

29. The method of claim **28** comprising counter-doping the first portion or the second portion at a second predetermined level.

30. The method of claim **29** wherein the first predetermined level of doping does not exceed the second predetermined level of doping.

31. The method of claim **1** further comprising forming a metal silicide layer over the semiconductor region.

32. The method of claim **1** wherein the surface of the semiconductor substrate has a substantially (100) crystallographic orientation.

33. The method of claim **1** wherein the dielectric region comprises a sidewall having an angle relative to the semiconductor substrate, the angle ranging from about 60° to about 90°.

34. The method of claim **33** wherein the semiconductor substrate has a <110> crystallographic plane, the sidewall being substantially aligned therewith.

35. The method of claim **33** wherein the semiconductor substrate has a <100> crystallographic plane, the sidewall being substantially aligned therewith.

* * * * *